This question paper contains 4 printed pages.]

1779 *Your Roll No. .....*

B.Sc. (Hons.) Computer Science / I Sem. A

Paper 104 – DIGITAL ELECTRONICS

(Admissions of 2001 and onwards)

Time : 3 Hours *Maximum Marks : 75*

(Write your Roll No. on the top immediately on receipt of this question paper.)

*Attempt **all** questions. Parts of a question must be answered together.*

1. (a) If $(210)_x = (36)_{10}$, Find the value of x. 2

(b) Perform the following operations using signed Arithmetic 3

(i) $(346)_8 - (655)_8$ (use 7's complement)

(ii) $(256)_{10} - (-52)_{10}$ (use 2's complement)

(c) If Octal codes are used to represent 12-bit addresses, then, 3

(i) How many octal digits are required ?

(ii) What is the range of addresses in octal ?

[P.T.O.

(iii) How many memory locations are there ?

2. (a) Show that positive logic AND gate is same as negative logic OR gate. 2

(b) Convert the following function into two canonical forms :

$$U = (x + \bar{y} + \bar{w} + z)\ (wy + y + \bar{w} + z)$$ 3

(c) The state of a 12 bit register is 0|0||00|0|||.
What is its contents if it represents :

(i) three decimal digits in BCD

(ii) three decimal digits in excess 3 code

(iii) three decimal digits in 2421 code. 3

3. (a) Minimize using Quine Mc-cluskey method. Determine the essential prime implicants.
F (A, B, C, D, E) = Σm (0, 1, 5, 8, 11, 12, 14, 16, 20, 21, 25, 27, 28, 30, 31)
and Σd (2, 7, 13, 22, 23) 7

(b) Design a combinational circuit that inputs a 4 bit number and generates its 4-bit 2's complement. 7

(c) Prove that $x \oplus 1 = x'$ and $x \oplus 0 = x$. 2

4. (a) Design a circuit for a 3-bit magnitude comparator. 5

(b) Implement the following function using a Multiplexer

$F(A, B, C, D) = \Sigma(2, 3, 5, 6, 8, 9, 11, 14, 15)$ 5

(c) What do you understand by race condition of a J.K. Flip Flop ? What are the possible pollutions ? 5

(d) Construct a T flip flop from a D flip flop. 2

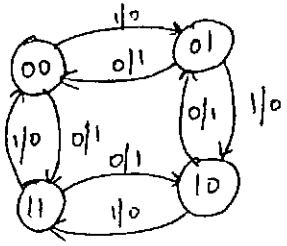
5. (a) It is necessary to formulate the Hamming code for four data bits D_3, D_5, D_6 and D_7 together with three parity bits P_1, P_2 and P_4. 6

(i) Evaluate the 7-bit composite code word for the data word 0010.

(ii) Evaluate three check bits C_4, C_2 and C_1 assuming no error.

(iii) Assume an error in bit D_5 during writing into memory. Show how the error in the bit is detected and corrected.

(b) Design the sequential circuit specified by the following state diagram using T-flip flops. Explain the function that the circuit performs. 7



(c) Determine the state diagram for the sequential system described by the following expressions :

$$s(t+1) = \begin{cases} s(t) & \text{if } x = a \\ (s(t)+1) \text{ moel } 5 & \text{if } x = b \\ 2 & \text{if } x = c \end{cases}$$

$$z(t) = \begin{cases} 0 & \text{if } s(t) \text{ is even} \\ 1 & \text{otherwise} \end{cases}$$

the system has five states. 4

6. (a) Differentiate between critical race and non critical race of an asynchronous sequential circuit. 3

(b) Give the internal organization of 64 × 4 RAM. 3

(c) Describe the conditions at each input and output when the data word 1110 is to be written into the address location 01001. 3