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1782 *Your Roll No. .....*

B.Sc. (H) Computer Science / (II Sem.) A

Paper 202– COMPUTER SYSTEM ARCHITECTURE

(Admissions of 2001 and onwards)

Time : 3 Hours *Maximum Marks : 75*

(Write your Roll No. on the top immediately on receipt of this question paper.)

*Attempt **all** questions. Parts of a question must be answered together.*

1. (a) Show the representation of +8 and -7 in:

(i) Signed magnitude representation

(ii) Signed 2's Complement representation 2

(b) Describe the address sequencer for the micro programmed control unit having control memory of 128 words. There are 4 status bits in the system. Length of microinstruction is 20 bits out of which 9 bits are used for micro operations. 5

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(c) What are the basic elements of bus design? How they differentiate and classify buses? 5

2. (a) What should be the size of memory address register (MAR) and memory data register (MDR) if RAM has a capacity of storing capacity 1M words and word size is 16-bit. 2

(b) Define fetch, decode phases of instruction cycle. Describe the sequence of micro-operation and flowchart showing register transfer statement of various phases of typical CPU. 5

(c) The memory unit of computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of the 15 addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if instruction is stored in one memory word. 5

3. (a) What are the two instructions needed in the basic computer in order to set the E-flip flop to 1 ? 2

(b) What is the purpose of an addressing mode? An instruction is stored at location 300 with its address field at location 301. The address field has the

values 400. A processor register R1 contains the number 200. Evaluate the effective address (EA) if the addressing mode of the instruction is

(i) Direct

(ii) Relative

(iii) Immediate. 6

(c) A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer. 4

4. (a) Show the step-by-step multiplication process using Booth's algorithm for (+23) ×(+19). Assume 8-bit registers that hold the numbers. 5

(b) Derive an expression for a speed up factor S of K-segment instruction pipeline and shows that the speed-up factor is approximately equal to number of segment in pipeline. Also draw a space time diagram of a six segment instruction pipeline. 5

(c) Give the differences between isolated I/O and memory-mapped I/O. 2

5. (a) Give and explain Direct Memory Access (DMA) I/O operation with the help of block diagram. 5

(b) What are the different kind of mapping used between main memory and cache memory? Explain in detail about direct mapping. 5

(c) Give the differences between hardwired and micro programmed control architectures. 2

6. (a) Give I/O channel architecture with the help of diagram. 6

(b) What are the main differences between CISC and RISC class of computer system architectures? 3

(c) Explain branch and save address (BSA) instruction. 2

(d) Give the utility of Replacement algorithms w.r.t. mapping between main memory and cache memory. How performance of cache is decided? 4