This question paper contains 4+2 printed pages]

Your Roll No. .....

1941

B.Sc. (H) Computer Science/(II Sem.) **C**

Paper 202—COMPUTER SYSTEM ARCHITECTURE

(Admissions of 2001 and onwards)

Time : 3 *Hours* *Maximum Marks* : 75

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question No. 1 is compulsory. Attempt any *four* questions from question numbers 2 to 7.

Section A

1. (*a*) If total memory space accessed by the CPU is 16K × 32, how many bits are required in its program counter (PC) and data register (DR) ? 2

(*b*) Draw the timing diagram assuming SC is cleared to zero at T_4, if C_7 is active :

$$C_7 T_4 : SC \leftarrow 0$$ 3

P.T.O.

(*c*) Explain the usage of FGI and FGO flip-flops. How do they work in conjunction with an IEN flip-flop ? 4

(*d*) Show how a 9-bit microoperation field in a microinstruction can be divided into subfields to specify 46 microoperations. How many microoperations can be specified in one microinstruction ? 4

(*e*) How can the opcode of an instruction be used to obtain the starting address of a micro-program routine ? 3

(*f*) What is a loop buffer ? What are the benefits of using a loop buffer ? 4

(*g*) Differentiate between burst transfer and cycle stealing. 3

(*h*) Why is mapping required between Cache and Main memory ? 3

(*i*) Differentiate between Read-modify-write and Read-after-write types of data transfer. 4

(*j*) Compute $(15)_{10} \times (13)_{10}$ using 2's complement division. Assume 5 bit registers that hold signed numbers. 5

Section B

2. (*a*) Give the sequence of register transfer statements starting from execution phase :

(*i*) Branch if AC positive and non-zero

(*ii*) Exchange AC and Memory content. 2

(*b*) A control memory in a microprogrammed control unit has 4096 words of 24 bits each : 3

(*i*) Give the number of bits in CAR

(*ii*) Specify the inputs to two MUX used in the system.

(*c*) Write a symbolic microprogram for fetching and execution of a BRANCH instruction. 5

3. (*a*) What are the characteristics of RISC and CISC processors ? How is a RISC processor better than a CISC processor ? Justify your answer. 3

(*b*) What is cache coherency ? Explain various approaches to maintain cache coherency in a multiprocessor system. 4

(*c*) List and define any *three* factors that determine the number of addressing bits required in an instruction. 3

4. (*a*) List and explain the different types of I/O commands received by an I/O processor when it is addressed by a processor. 5

(*b*) What design issues arise in implementing an interrupt driven I/O ? Explain any *two* techniques adopted to resolve these issues. 5

5. (*a*) Define the following terms in the context of a memory component :

(*i*) Access time

(*ii*) Memory cycle time

(*iii*) Transfer rate. 3

(*b*) How does cache make use of spatial locality and temporal locality while using locality of reference principle ? 2

(*c*) Describe Set Associative mapping with the help of an example. 5

6. (*a*) For an instruction cycle, draw a six-segment pipeline and its timing diagram. Assume that the 3rd instruction is a branch instruction. 5

(*b*) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed-up ratio of the pipeline for 100 tasks. What is the maximum achievable speed-up ? 5

7. (*a*) Explain Direct Memory Access with the help of a block diagram of DMA controller. 5

(*b*) Let the address stored in the program counter be 202. The instruction stored in 202 has an address part 501. The operand needed to execute the instruction is stored in the memory location 611. An index register contains 723. Illustrate the relationship between these various quantities if the addressing mode of the instruction is :

(*i*) direct

(*ii*) indirect

(*iii*) relative

(*iv*) indexed

(*v*) immediate. 5