[This question paper contains 4 printed pages.]

Sr. No. of Question Paper : 842 **E** **Your Roll No.....**

Unique Paper Code : 234203

Name of the Course : **B.Sc. (H) Computer Science**

Name of the Paper : Computer System Architecture (CSHT–204)

Semester : II

Duration : 3 Hours Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Attempt **all** questions from **Section A.**
3. Attempt any **four** questions from **Section B.**
4. Attempt all parts of a question at one place.

SECTION – A

1. (a) Define fetch, decode and execute phases of the instruction cycle in a basic computer. State the sequence of microoperations using register transfer statements. (5)

   (b) Write an assembly language program to subtract one number from the other. (5)

   (c) Draw the diagram of the micro-program sequencer of a basic computer and explain its working. (5)

   (d) Convert the following arithmetic expressions from infix to Reverse Polish Notation (RPN) :

   (i) A+B*C+D*E+F

P.T.O.

(ii) A+B*[C*D+E/(F+G)] (5)

(e) The time delay of four segments in a pipeline are as follows :

t_1 = 50 ns, t_2 = 30 ns, t_3 = 95 ns and t_4 = 45 ns. The interface registers delay time t_R = 5 ns. How long would it take to add 100 pairs of numbers in the pipeline ? A non pipeline system takes t_N = 90 ns to process a task. Determine the speedup ratio of the pipeline for 100 tasks. (5)

(f) Differentiate between isolated and memory mapped I/O. Give advantages and disadvantages of each. (5)

(g) Explain direct mapping in cache memory with the help of an example. Draw a well labeled diagram of the process. (5)

SECTION – B

2. (a) How is an interrupt processed in a computer ? Explain the changes that occur in memory and CPU registers before and after the occurrence of the interrupt. (5)

(b) Show the contents (in hexadecimal) of registers PC, AR, DR. IR and SC of the basic computer when an ISZ instruction is fetched from the memory and executed. The initial content of PC is 7FF. The content of memory at address 7FF is EA9F. The content of memory at address A9F is 0C35. The content of memory at address C35 is FFFF. Show the contents of registers in a tabular format. (5)

3. (a) What are the characteristics of I/O channels ? Draw and explain Multiplexor channel. (5)

(b) Let the address stored in the program counter be X1. The two word instruction stored in X1 has an address part X2. The operand needed to execute the instruction is stored in the memory location X3. An index register

contains X4. Calculate the effective address of the operand if the addressing mode of the instruction is :

(i) immediate

(ii) direct

(iii) indirect

(iv) relative

(v) indexed (5)

4. (a) Write a symbolic micro program for fetching and execution of an EXCHANGE instruction. (5)

(b) A digital computer has *a* memory unit with a capacity of 16, 384 words of 40 bits each. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no mode bit present). Two instructions are packed in one memory word and a 40 bit Instruction Register (IR) is available in the CPU. Formulate a procedure for fetching and executing an instruction for this computer. (5)

5. (a) Draw a six-segment pipeline and its timing diagram for an instruction cycle. Assume that the 3rd instruction is a branch instruction. (5)

(b) Write two assembly programs to evaluate the expression X = (A + B) * (C+D) using three and two address instructions respectively. (5)

6. (a) List the elements of bus design. Differentiate between synchronous and asynchronous timing with the help of diagrams. (5)

(b) Draw the diagram of a DMA module and explain its functions. (5)

7. (a) Explain the working of PCI bus in a typical desktop system. (5)

(b) A two way set associative memory uses blocks of four words. The cache can accommodate a total of 2048 words from the main memory. The main memory has a size of 128K × 32 bits. Design the cache structure and explain how the CPU generated address is interpreted. (5)