1982 B.Sc (Hons.) Computer Science (Vth SEM) (Old Course)
Paper: CS– 502 Computer Networks

C

Time: 3 Hrs. **Max Marks: 75**

All questions in Section-A are compulsory.
Attempt any Four questions in Section-B.

Section – A (Compulsory)

Q 1. a) Distinguish between the following: - 2 + 2

i) In-band signaling and Out-band signaling

ii) Baseband and Broadband

b) With respect to ISO-OSI model, name the layer(s) in which the following devices operate: 5

i) Application Gateway

ii) Firewall

iii) Hub

iv) Router

v) Bridge

c) What signal-to-noise ratio is needed to put a T1 carrier on a 50-kHz line? 3

d) List any three built-in HTTP request methods. 3

Q 2. a) What is multipath fading? Out of the following techniques, explain the one that provides resistance to the multipath fading. 2+2

i) Direct sequence spread spectrum

ii) Frequency hopping spread spectrum

b) How is Frame Relay different from X.25? Explain. 4

c) Briefly explain TCM. 2

Q 3. a) Consider a class C IP addresses 192.205.92.142/22. Identify the following: 2

i) Number of hosts within a subnet

ii) Number of subnets

b) What is a DC component? 2

c) Describe the steps in brief to convert analog signal to digital signal. 4

d) A bit string 10111100111110111111110, needs to be transmitted at the Data Link Layer. What is the string actually transmitted after bit stuffing? 2

Section – B (Attempt any 4 Questions)

Q 4. a) Why do you think that an Ethernet frame should have a minimum data size? 2

b) Name and explain the algorithm that is used to reduce collisions in Ethernet. 1+3

c) What are the three switching techniques? Explain each of them. 1+3

Q 5. a) Compare and contrast the datagram subnet and virtual circuit subnet. 4

b) Describe the three categories of services provided by ISDN. 3

c) What is the size of ATM cell? How are ATM cells multiplexed? 1+2

Q 6. a) Explain the TCP segment Header with the help of a diagram. 7

b) What is loopback address and why it is used for? 1+2

Q 7. a) Why sliding window protocol is better than Stop and Wait protocol? Explain. 4

b) A bit stream 10011101 is transmitted using the CRC method. The generator polynomial is $x^3 + 1$. Show the bit string transmitted. Suppose the third bit from the left is inverted during transmission. Show that this error is detected at the receiver's end. 3+3

Q 8. a) Consider the bit stream 1100101100111001011. Give the waveform for the following:- 2+2

i) Manchester encoding.

ii) Differential Manchester encoding.

b) Transport layer is responsible for process to process delivery of data. Justify. 3

c) Write short note on the Bluetooth. 3

Q 9. Differentiate between the following: 10

i. FDDI and Token Ring

ii. ICMP and ARP

iii. BOOTP and DHCP

iv. NRZ-L and NRZ-I

v. Store and forward switches and Cut through switches

1983

B.Sc. (Hons) Computer Science 5th Semester (Old Course) C

Paper No: 503 **Paper name: Microprocessors**

Duration: 3 Hours Maximum Marks: 75

INSTRUCTIONS:

Paper is divided in two sections as **Section A** and **Section B.**
Question No. 1 is compulsory and attempt any ***four*** **questions** from **Section B.**
Parts of a question should be attempted together.

Section A

1. (a) Describe program visible and program invisible registers of microprocessor 8086. (4)

   (b) What is the purpose of the GTDR in 80286 Microprocessor? (2)

   (c) Write three instructions using register addressing mode. (3)

   (d) Suppose that DS=1300H, SS=1400H, BP=1500H and SI=0100H. Determine the address accessed by each of the following instruction, assuming real mode operation:

   (i) MOV EAX, [BP+100H]

   (ii) MOV AL, [BP+SI-100H]

   (iii) MOV AL, [SI-01004] (6)

   (e) Which is more efficient, a MOV with an OFFSET or an LEA instruction? (3)

   (f) What does the INT 21H accomplish if AH contains a 09H? (3)

   (g) What are special-purpose registers? Discuss different types of flags used in EFLAG register. (4)

   (h) What is the purpose of the following pins on memory component?
   (i) $\overline{CE}$
   (ii) $\overline{OE}$
   (iii) WE (3)

   (i)The NMI interrupt automatically vectors through which vector type number? (3)

   (j) Explain the operation of the test pin and the WAIT instruction. (2)

   (k) What is the purpose of status bits S3 and S4 in 8086/8088 microprocessors? (2)

Section-B

2. (a) Describe following addressing mode with the help of examples
   (i) Base-Index addressing mode
   (ii) Stack memory addressing mode (4)

   (b) Explain the programming model of the Intel 8086 through Pentium 4. (6)

3. (a) Give the functions of the following pins of 8086 microprocessors:
   (i) $IO/\overline{M}$
   (ii) $\overline{WR}$
   (iii) $\overline{INTA}$
   (iv) HLDA
   (v) DEN
   (vi) HOLD (6)

   (b) What is protected mode memory addressing? Show difference between descriptors of 80286 and 80386. (4)

4. (a) Explain READ bus cycle and WRITE bus cycle of 8086 with the help of timing diagram. (5)

   (b) If $\overline{BHE}$ is a logic 0 and A_0 is at a logic 1 then which memory bank are selected. (2)

   (c) Why are both $\overline{BHE}$ and $\overline{BLE}$ (A0) ignored in a 16-bit port address decoder in I/O interface with Intel family microprocessor. (3)

5. (a) What are memory banks? Explain the most effective way to handle bank selection. (6)

   (b) What information appears on the address/data bus of the 8086 while ALE is active? (2)

   (c) Which microprocessor pins are used to request and acknowledge a DMA transfer? (2)

6. (a) Describe the basic functioning of programmable peripheral Interface (PPI) 82C55 chip. (5)

   (b) Explain three status registers available for readable in 8259A chip . (5)

7. (a) Give the detailed functioning of 8237 Direct Memory Access(DMA) controller in 8086 microprocessor. (6)

   (b) Discuss execution units of Pentium microprocessor. (4)