

- (e) Why is an anisotropic crystalline silicon wafer preferred over a isotropic amorphous silicon wafer in device fabrication ? (3×5)
2. (a) Define Effective Mass and derive an expression for density of States.
- (b) Using the concept that electrons in solids follow Fermi-Dirac statistics, obtain the expression for Electron Concentration in the Conduction Band.
- (c) Find the Fermi energy level in intrinsic semiconductor. (6,6,3)
3. (a) Derive the current-voltage relation in an infinitely long diode.
- (b) Explain the difference between Zener and Avalanche breakdown mechanism.
- (c) For Fig. 1, indicate which side is p-type and which side is n-type. What reverse voltage would be required for Zener break-down ? (8,4,3)

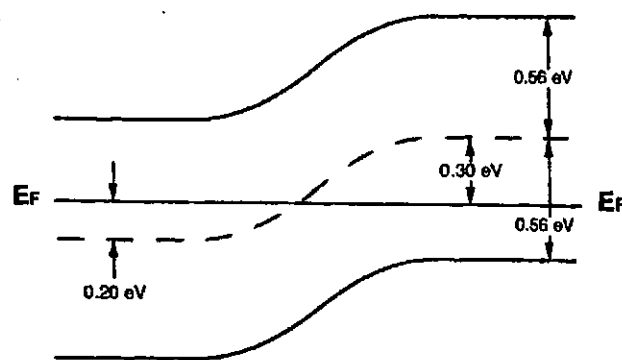


Figure 1

4. (a) Using the transistor current relation $I_E = I_B + I_C$, derive a relationship between I_{CEO} and I_{CBO} (notations having usual meaning).
- (b) If two points on the I-V characteristics marking the saturation region (0,4 mA) and cut-off region (20 V,0) are given, what point in the active region is best suited for the transistor operation? Justify your answer.
- (c) Based on the I-V characteristics discuss why the CE mode is popular? Also, state and justify the applications suited for transistors in their CB and CC mode. (6,3,6)
5. (a) Sketch the basic structure of a Uni-Junction Transistor (UJT) and explain its I-V characteristics.
- (b) Draw the doping profile of a SCR. Based on this, explain its I-V characteristics. (8,7)
6. (a) Explain the operation of enhancement mode-MOSFET and draw its I-V characteristics.
- (b) From the output I-V characteristics of a JFET, explain how it can be used as a voltage controlled resistance?
- (c) Define channel conductance and transconductance of a FET. (8,4,3)
7. (a) Compare the ion implantation technique and the thermal diffusion technique used for selective introduction of dopant atoms into the substrate.
- (b) Define resolution, registration and throughput in lithographic process.

- (c) Discuss the various steps involved in the fabrication of a CMOS structure with the help of diagrams. (4,3,8)