[This question paper contains 6 printed pages.]

6001 *Your Roll No.* .....

B.Sc. (H) ELECTRONICS / III Sem. B

Paper – ELHT-301

Digital Electronics

(Admissions of 2010 and onwards)

Time : 3 Hours *Maximum Marks : 75*

(Write your Roll No. on the top immediately on receipt of this question paper.)

Attempt **Five** *questions in all including Q. No.* **1** *which is compulsory. Non-Scientific calculator is allowed.*

1. (a) Find the complement of function F, using DeMorgan's theorem.

$$F = (AB + C)(D + A'B) + \overline{AB'D} \quad (3)$$

(b) Implement A□ B□ C using a 4×1 Multiplexer. (3)

(c) Define the terms Propagation Delay, Data Hold up time and set up time. (3)

P.T.O.

(d) For J-K flip flop, give the excitation table and transition function $Q(t+1)$. (3)

(e) Give the three major differences between SRAM and DRAM. (3)

2. (a) It is necessary to formulate the Hamming Code for 4-bits Data (D_3, D_5, D_6 & D_7) together with three parity bits P_1, P_2 and P_4.

(i) Evaluate the 7-bit composite code word for the data word 0010.

(ii) Evaluate three check bits C_4, C_2 and C_1 assuming no error.

(iii) Assume an error in bit D_5. Show how the error in the bit D_5 is detected and corrected. (6)

(b) Simplify the following Boolean Expression to a expression with minimum number of literals.

$$(X'Y' + Z)' + Z + XY + WZ \qquad (4)$$

(c) Add -17.34_{10} and -25.68_{10},

using 2's complement system of binary number representation with 8 bits in integer part and 4-bits in fractional part. (5)

3. (a) Data from one of the four different input sources is get connected to one output line. Which device will perform this operation ? Give the circuit diagram of the device. (4)

(b) Give the circuit diagram of a 3 bit parallel adder/ subtractor circuit which should add when the control line "SUB", is Low and subtract when it is high. (3)

(c) Minimize the following boolean function F, using Quine McCluskey Method.

$$F = \pi(0, 2, 4, 7, 10, 12, 14)$$ (8)

4. (a) Analyse the following sequential circuit with D-flip flop, giving

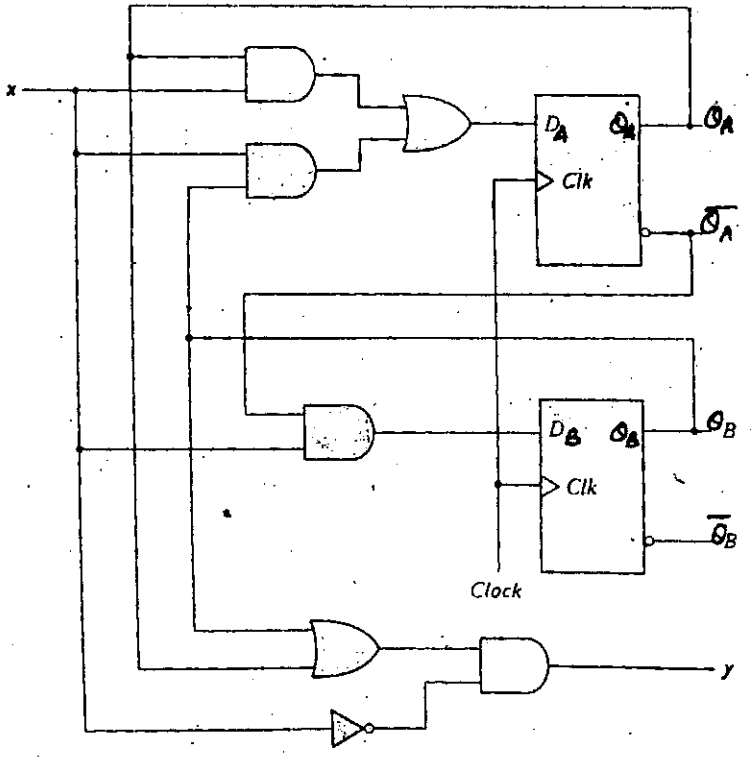
(i) Expression for flip flop inputs D_A and D_B.

(ii) Transition functions $Q_A (t + 1)$ and $Q_B (t + 1)$.

(iii) Expression for output, y.

(iv) State Table.

(v) State Diagram. (8)



(b) Explain with Diagram the working of a 4 Bit Bi-directional Shift register. (5)

(c) Describe the Race around condition. (2)

5. (a) Draw the circuit of a MOD-6 asynchronous Down counter, using Positive edge triggered JK flip flops having asynchronous clear and preset inputs. Give the waveforms at the output of each flip flop. (5)

(b) Give the circuit diagram and truth table of SR latch using NOR gates. (2)

(c) Design a type T-counter that must go through states 0, 2, 4, 6, 0 if control line X is high and through states 1, 3, 5, 7, 1 if control line X is low. Give the state diagram, state table and circuit diagram. (8)

6. (a) Determine the value of X, Y and Z

$$(X)_2 = (Y)_8 = (Z)_{10} = (SDC)_{16} \quad (3)$$

(b) Give the circuit diagram of totem-pole output of TTL NAND gate and explain its functioning. (5)

(c) Simplify the following Boolean function F, using five variable K-Map and implement the simplified function using NAND gates.

$$F(A, B, C, D, E) = \Sigma(0, 1, 4, 5, 16, 17, 21, 25, 29) \quad (7)$$

7. (a) Design a diode matrix ROM for Conversion of a single digit BCD to Excess-3 code. (8)

(b) Explain the R/ZR ladder network method for a 4-bit D to A convertor. (5)

(c) Each step of an 8 bit D/A convertor represents 0.2V. What do the following code represents in Analog.

00011101 (2)