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Sr. No. of Question Paper : 8745

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Roll No.....

Unique Paper Code : 251301

Name of the Paper : ELHT-301 : Digital Electronics

Name of the Course : B.Sc. (H) Electronics / Computer Science

Semester : III / I

Duration : 3 Hours

Maximum Marks : 75

(Write your Roll No. on the top immediately on receipt of this question paper.)

Instructions for candidates

Attempt five Questions in all.

Question.No:-1 is compulsory.

All Questions Carries equal Marks.

1. Attempt any five of the following.

a) Convert

(i) $B3D8_{16}$ into Decimal.

(ii) 1100.11_2 into Decimal.

(iii) 1993_{10} into Octal.

b) Subtract 23_{10} from 39_{10} using 2's complement arithmetic.

c) Implement AND,OR,XOR using NOR gate.

d) Explain $A + B\bar{C} + AB\bar{D} + ABCD$ to Minterms and maxterms.

e) Draw the AND-OR gate implementation of the following function after simplifying

$$F(A,B,C,D) = \sum m(0,2,5,6,7,8,10)$$

f) Implement SR FLIP-FLOP using D FLIP-FLOP

g). Differentiate between EPROM and EEPROM.

3x5

2. a). Draw the circuit diagram of standard TTL NAND gate and explain it.

b). Design a 4 input priority encoder with input $D_0D_1D_2D_3$. D_0 having highest priority, provide an output V to indicate that atleast one of the inputs is present.

c). Perform the following decimal addition using BCD arithmetic

$$27+78$$

6,6,3

P.T.O.

- 3 a). Design a 4-Bit Adder-Subtractor circuit and explain its working.
 b). Reduce the following expression to the simplified POS and SOP form

$$F = \sum m(6,9,13,18,19,25,27,29,31) + d(2,3,11,15,17,24,28)$$
- c). Implement Half-Adder using universal Logic gate. 5,7,3
4. a). Implement the following function

$$F(A,B,C,D) = \sum m(0,1,3,4,8,9,15)$$
 using 8:1 MUX
 b). Implement a Full adder using DECODER
 c). Design a 1:4 Demultiplexer and explain its working with Truth Table. 5,5,5
5. a). Design a universal shift register using MUX and explain working.
 b). Draw and explain the working of a +ve edge triggered JK Flip-Flop. What is meant by the race around problem in Flip-Flop. How does master slave configuration help in solving the problem. 7,8
6. a). Explain advantages and limitations of ripple counter. Design a MOD -10 asynchronous up-counter using +ve edge triggering.
 b). Design and Implement a BCD counter using JK Flip-Flop. Is the counter self starting? 8,7
7. a) Explain the working of 4-bit R-2R Ladder DAC.
 b). What are static and Dynamic RAMS? Discuss their merits and demerits and area of application.
 c). For a 4-bit Binary ladder DAC the input labels are 0=0V and 1=10V. Find
 (i) Output voltage corresponding to an input of 1011
 (ii) Full scale output voltage of the ladder 6,7,2