This question paper contains 2 printed pages. **Your Roll No. .....**

Sl. No. of Ques. Paper : **2050** **GC-3**

Unique Paper Code : **32511303**

Name of Paper : **Core Paper II Digital Electronics and VHDL**

Name of Course : **B.Sc. (Hons.) Electronics under CBCS**

Semester : **III**

Duration : **3 hours**

Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

*Attempt **five** questions in all. Question No. 1 is compulsory.*

1. Attempt any **five** parts:
   (a) Express $(84)_{10}$ in the following codes: (i) Gray, (ii) Octal, (iii) Hexadecimal. 3
   (b) Subtract 14_{10} from 46_{10} using 8 bit 2's complement arithmetic. 3
   (c) Determine the complement of function, $y = A(BC' + BD' + CD')$ 3
   (d) What are asynchronous inputs in Flip Flops? Why are they called asynchronous? 3
   (e) Explain the difference between edge triggered and level triggered Flip Flops. 3
   (f) What is concurrent signal assignment statement? Give one example. 3

2. (a) Express the Boolean function, F = AB + A'C as sum of minterms and product of maxterms. 5
   (b) Design and explain the working of 4-bit ADDER/SUBTRACTOR circuit. 6
   (c) Compare TTL and CMOS logic families. 4

3. (a) Minimize the logic function given below using Karnaugh map:
   $F = \Sigma m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$
   Implement the minimized expression using universal logic gates. 7
   (b) Implement a full subtractor using a 3 to 8 decoder and logic gates. 4
   (c) Design a 8×I MUX using two 4×I MUX. 4

4. (a) Design a MOD 10 asynchronous counter using positive edge triggered T Flip Flops. 6
   (b) Design a synchronous counter that goes through the states 6, 4, 2, 1, 6, ... Check whether the counter is self starting. 7
   (c) Draw the logic diagram of a parallel-in parallel-out shift register that stores the binary word 1101. 2

5. (a) Explain briefly different data types in VHDL. 4
   (b) Write a VHDL code to implement 4×1 Multiplexer. 7
   (c) Explain the execution of the following process statement:

```
Process (A)
        variable EVENTS_ON_A : INTEGER : = –I;
begin
        EVENTS_ON_A := EVENTS_ON_A+l;
end process;
```

4

P.T.O.

6. (a) Design a 4 bit shift register using D Flip Flop. Explain how it can be modified to obtain ring counter. 5

(b) Using excitation table, convert a T Flip Flop to a JK Flip Flop. 5

(c) Design a BCD to binary code converter. 5

7. (a) Define and explain the following terms using timing diagram:

(i) Setup time

(ii) Hold time. 5

(b) Differentiate between PLA and PAL. 6

(c) Name four important characteristics of digital IC logic families which determine their performance. 4