Your Roll No. .....

This question paper contains 2 printed pages.

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Sl. No. of Ques. Paper : **947**
Unique Paper Code : **251301**
Name of Paper : **Digital Electronics (ELHT-301)**
Name of Course : **B.Sc. (Hons.) Electronics / Computer Science**
Semester : **III**
Duration : **3 hours**
Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Q. No. 1 is compulsory. Attempt five questions in all.
Use of scientific calculator is allowed.

1. (a) Given that $16_{10}=100_b$ find the value of b. 3

(b) Implement a half adder using a 4×1 multiplexer. 3

(c) Give the logic implementation of a 32×4 bit ROM using a decoder of suitable size. 3

(d) Describe the Race around condition with reference to JK flip flop. 3

(e) Define the terms:

(i) Figure of Merit

(ii) Noise Margin. 3

2. (a) Express the following functions as sum of Minterms and product of Maxterms: 6

$F(A, B, C, D)= \overline{B}D+\overline{A}D+B\overline{D}$

(b) Given the 8-bit data word 01011011, generate the 12-bit composite word for the Hamming code that corrects and detects single errors. 5

(c) Design a combinational circuit with three inputs x, y and z and three outputs A, B and C. When the binary input is 0, 1, 2 or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is two less than the input. 4

3. (a) Design a 4 bit priority encoder with D_0 having lowest priority and D_3 having highest priority. 6

(b) Using the Quine-McCluskey method, obtain the minimal expression for: 5

$f=\sum m(6, 7, 8, 9)+d(10, 11, 12, 13, 14, 15)$. 4

(c) Implement a half subtractor using a 2 to 4 line decoder.

P. T. O.

4. (a) A synchronous sequential machine has a single control input X, a clock and two outputs A and B. The clock triggers AB to change state from 00 to 01 to 10 to 11 and back to 00, if input X is 1 and the output remains in its present state if X is 0. Draw the state diagram, state table and implement using T flip-flops. 7

(b) Draw the circuit of a 4 bit parallel adder-subtractor using block diagram. 5

(c) Distinguish between combinational and sequential circuits. 3

5. (a) Design a type J-K counter that goes through states 0, 1, 2, 4, 0 ..... . Is the counter self-starting? Give the state diagram, state table and circuit diagram. 7

(b) Implement the logical expression for difference of a full subtractor using a 8×1 MUX. 4

(c) Convert an SR flip-flop to JK flip-flop using excitation table. 4

6. (a) Design a 4-bit BCD to gray code converter. 5

(b) Draw the block diagram of 4-bit Bidirectional shift register. 5

(c) Explain working of positive logic CMOS NAND gate. 5

7. (a) With the help of block diagram explain the working of successive approximation ADC. 6

(b) A 6-bit DAC has a step size of 50 mV. Determine the full scale output voltage and the percentage resolution. What would be the analog output if digital input is 100000? 5

(c) Distinguish between:

(i) SRAM and DRAM

(ii) PROM and EEPROM. 4