This question paper contains **4** printed pages]

Roll No. | | | | | | | | | | |

S. No. of Question Paper : **1584**

Unique Paper Code : **222204** **C**

Name of the Paper : **Digital Electronics (PHHT-206)**

Name of the Course : **B.Sc. (Hons.) Physics**

Semester : **II**

Duration : **3 Hours** Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Attempt all *five* questions.

1. Attempt any *five* of the following : 5×3=15

   (*a*) Draw the circuit for 4-bit odd parity generator.

   (*b*) Define Common Mode Rejection Ratio (CMRR) for an Op-amp.

   (*c*) Define accuracy and resolution of D/A convertor.

   (*d*) How many flip-flops are required to produce divide by 64 counters ?

   (*e*) Define *set up time* and *hold time* in flip-flops.

P.T.O.

(*f*) Prove that :

$$(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C).$$

(*g*) Subtract 20.25_{10} from 34.75_{10} using 2's complement method.

(*h*) Draw the circuit diagram of clocked RS FF using NAND gates only.

2. (*a*) Draw the circuit diagram of Astable multivibrator using IC555 timer and explain its operation. Obtain the expression for frequency of output waveform. Determine the condition under which 50% duty cycle is possible. 7½

(*b*) For a 4-bit R-2R ladder D/A converter the input levels are logic 0 = 0 V and logic 1 = +10 V, find the :

(*i*) Output voltage caused by each bit.

(*ii*) Full scale output voltage of a ladder.

(*iii*) Percentage resolution. 7½

Or

Draw the block diagram of CRO. Explain the function of :

(*i*) Time base generator

(*ii*) Delay line

(*iii*) Aquadag Coating. 7½

3. (*a*) What is the difference between open loop and closed loop gain of an op-amp ? Plot transfer characteristics of inverting Amplifier of gain of 10 if Op-Amp is given dual power supply of ±12 volts. 7½

(*b*) Using Operational Amplifier, design a circuit for performing the following operation :

$$V_0 = -(V_1 + 4V_2 + 2V_3)$$

where V_0 is the output voltage; V_1, V_2 and V_3 are the input voltages. 7½

Or

Describe how an operational amplifier is used to perform the mathematical operation of differentiation. What would be the expression for output if the input is given by :

$$V_{in} = V \sin \omega t.$$ 7½

4. (*a*) Minimize the following logic function using K-map :

$$F(A, B, C, D) = \Sigma(0, 4, 7, 8, 10, 13, 15) + \Sigma d(2, 5, 12).$$

Write the minimized Boolean expression in sum of product form and realize it using 2-input NAND gates only. 7½

(*b*) What is a multiplexer ? Implement the following function with 8 × 1 multiplexer :

$$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 4, 8, 11, 14, 15).$$ 7½

Or

What is a decoder ? Design a full adder circuit using a decoder and OR gates. 7½

P.T.O.

5. (*a*) Draw the circuit diagram of JK-FF using NAND gates and give its truth table. How JK flip-flop can be converted to D flip-flop and T flip-flop ? Explain with relevant block diagram ? Give *one* application of each of D flip-flop and T flip-flop. 7½

(*b*) Design a MOD-6 synchronous counter using block diagram of appropriate flip-flops. 7½

Or

Draw the circuit diagram of 4-bit bi-directional shift register. Explain its operation. 7½