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Roll No. | | | | | | | | | | |

S. No. of Question Paper : **938**

Unique Paper Code : **222204** **E**

Name of the Paper : **Digital Electronics (PHHT-206)**

Name of the Course : **B.Sc. (Hons.) Physics**

Semester : **II**

Duration : **3 Hours** Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Attempt all *Five* questions.

1. Attempt any *five* of the following : 5×3=15

(*a*) Obtain two input OR gate using NAND gates only.

(*b*) Draw pin-out diagram of Op-Amp 741 and define its slew rate.

(*c*) Define output offset voltage of an Op-Amp. How is this voltage reduced to zero in 741 ?

(*d*) Simplify the Boolean expression :

$$\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC + B.$$

(*e*) What is the minimum number of select lines required for selecting one out of 1024 input lines in a multiplexer ?

P.T.O.

(*f*) Differentiate between Synchronous and Asynchronous counters.

(*g*) What is advantage of JK flip-flop over RS flip-flop ?

2. (*a*) Draw the circuit of a basic differentiator using Op-Amp and obtain expression for its output. What are the drawbacks of basic differentiator ? What steps should be taken to overcome these ? 7½

(*b*) Derive an expression for the closed loop gain of Op-Amp 741 configured in non-inverting mode. What would be the output of this circuit if it has a gain of 30 for a d.c. input signal of 1.0 volt ? ($V_{CC} = \pm$ 15 volts). 7½

Or

Explain with suitable diagram the working of operational amplifier as an adder. 7½

3. (*a*) Design a logic circuit with a 4-bit input such that the output is HIGH whenever 2 and 3 input bits are HIGH and realize it using NAND gates. 7½

Or

Minimize the following logic function using Karnaugh map :

$$F(A, B, C, D) = \Sigma m(1, 3, 5, 9, 11, 15) + d(2, 10, 13)$$

Write down the minimized logic expression and realize it using NAND gates. 7½

(*b*) Describe the truth table of Half-Subtractor giving its circuit to explain Borrow and Difference. How to connect two half-subtractors together to make one full subtractor ? 7½

4. (*a*) Draw the circuit diagram of a Master-Slave JK flip-flop and explain how does it prevent racing ? 7½

(*b*) Draw circuit diagram of a modulo-8 ripple counter using negative edge-triggered JK flip-flops. Draw its output waveforms showing eight clock pulses. How to modify the circuit to make it modulo-5 counter ? 7½

Or

What are shift registers ? Explain with suitable block diagram, the working of a 4-bit serial-in serial-out shift register. 7½

5. (*a*) Draw the circuit diagram of an Astable multivibrator using IC555 and explain its operation. Derive an expression for frequency and duty cycle of the output waveform. Discuss the condition for 50% duty cycle. 7½

(*b*) For a 5-bit binary R-2R ladder D/A converter the input levels are 0 = 0 V and 1 = +10 V. Find :

(*i*) the output voltage caused by each bit

(*ii*) full scale output voltage of the 5-bit ladder

(*iii*) output voltage for the digital input 11010. 7½

Or

Draw block diagram of Cathode Ray Oscilloscope and explain how it is used to estimate voltage, frequency and phase of a sinusoidal wave. 7½