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Your Roll No.....

5187

B.Sc.Phy.Sc./III Sem. **B**

Paper CSPT 303 : COMPUTER SYSTEM ARCHITECTURE

(Admission of 2010 and onwards)

Time : 3 *Hours* *Maximum Marks* : 75

(Write your Roll No. on the top immediately on receipt of this question paper.)

All questions carry equal marks.

1. (A) Simplify the Boolean function F together with the don't care conditions *d* in : 5

(*i*) Sum of products form

(*ii*) Product of sum form

$F(w, x, y, z) = \Sigma(0, 1, 2, 3, 7, 8, 10)$
$d(w, x, y, z) = \Sigma(5, 6, 11, 15)$

(B) Using Boolean algebra, show that : 6

(*i*) $(A + B)' (A' + B') = 0$

(*ii*) $A + A'B + A'B' = 1$

(*iii*) $(BC' + A'D) (AB' + CD') = 0.$

P.T.O.

(C) Perform the arithmetic operations (+70) + (+80) and (–70) + (–80) with binary numbers in signed two's complement representation using 8-bits. 4

2. (A) In a basic computer some of the memory-reference instructions with their respective opcodes are as follows : 7

Symbol	Opcode	Description
XOR	000	Exclusive-OR to AC (Assuming computer can perform XOR)
SUB	001	Subtract memory from AC
XCH	010	Exchange AC and Memory

Give the sequence of register transfer statements needed to :

(*i*) Fetch and Decode the instruction.

(*ii*) Execute each of the above instruction.

(B) Construct a 16 × 1 line multiplexer with two 8 × 1 line multiplexers and one 2 × 1 line multiplexer. Use block diagrams. 5

(C) The following memory units are specified by the number of words times the number of bits per word. Specify the number of address lines, data lines and memory size in bytes : 3

(*i*) 16 M × 32

(*ii*) 4G × 64.

3. (A) What are flip-flops ? Differentiate between positive and negative edge-triggered flip-flops. 3

(B) Show how an SR flip-flop can be converted to a D flip-flop. 2

(C) What is a counter ? Why does the counter circuit usually employ JK or T flip-flops ? How many flip-flops will be complemented in a 10-bit binary counter to reach the next count after 1001100111. 5

(D) Draw the circuit diagram for 4-bit bidirectional shift register with parallel load. 5

4. (A) What is an instruction cycle ? Write the control function and micro-operations required to fetch, decode and execute LDA and BUN operations in the basic computer. 5

(B) The contents of PC in the basic computer is 3AF. The contents of AC is 7EC3. The contents of memory at address 3AF is 932 E. The contents of memory at address 32 E is 09AC and at 9AC is 8B9F. (Given the following codes : 1000 for AND, 1001 for ADD, 1010 for LDA). Show the binary operations that will be performed and give the contents of the registers PC, AR, DR, AC, IR and SC, the values of E and I flip-flops. 5

(C) Given the following expression : 5

$X = A - B + C^* (D + E)/(F + G * H)$

Write the required sequence of steps needed to evaluate the above expression using :

(*i*) Two address instructions

(*ii*) One address instructions.

5. Write short notes on any *three* : 5×3

(*i*) Interrupt cycle

(*ii*) Isolated *Vs.* Memory Mapped I/O

(*iii*) DMA

(*iv*) *Register* Indirect and Indexed Addressing modes.