This question paper contains 4 printed pages.]

5193H *Your Roll No. .....*

B.Sc. (Prog.) Physical Sciences / IV Sem. B

Paper ELPT-404

Digital Electronics

Time : 3 Hours *Maximum Marks : 75*

(Write your Roll No. on the top immediately on receipt of this question paper.)

*Attempt any **five** questions.*
All questions carry equal marks.

1. (a) Add 342 and 669 using BCD codes. 5

   (b) Add –23 and –39 using signed binary numbers. (2's complement). 5

   (c) Convert 121.375 in to equivalent Binary. 5

2. (a) Simplify the following expression using Boolean algebra:

   $Y = \overline{\overline{ABC} + \overline{AB} + \overline{BC}}$ 5

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(b) State duality theorem and show that the dual of an XOR is equal to its compliment. 5

(c) Obtain the truth table of the following function and express it in sum of minterms and product of maxterms:

$F(A,B,C,D) = \overline{B}D + \overline{A}D + BD$ 5

3. (a) Minimize the following Boolean expression using K - map and implement it using NAND gates only.

$F(A,B,C,D) = \sum m(0,3,4,5,7,9,12,13,14,15)$ 6

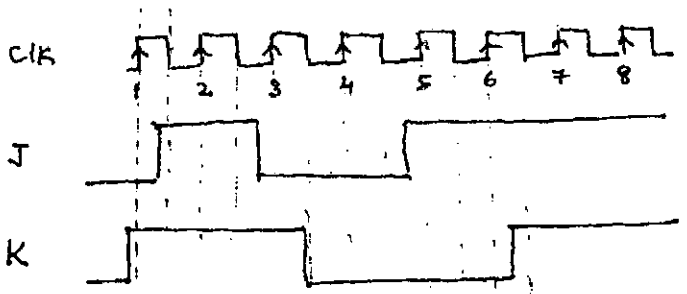
(b) Implement a full - adder with two half adders and an OR gate. 3

(c) Draw and explain the logic circuit diagram of 4–bit Adder - cum – Subtractor. 6

4. (a) Draw a logic circuit for binary to octal decoder. 7

(b) Construct a 16x1 MUX using two 8x1 and one 2x1 MUXs. Use block diagram only. 8

5. (a) Draw the logic circuit of an edge triggered J-K flip-flop and give its truth table. If the input waveforms for J and K are as given below, find the waveform for Q output. 8



(b) Draw the logic circuit of a Master – Slave J-K flip -flop and explain how it prevents race around condition. 7

6. (a) Draw the logic circuit of an asynchronous decade counter and explain its operation. 8

(b) Draw a circuit for a controlled left shift register for four bits and explain its working. 7

7. (a) Draw the circuit of a 4-bit Digital to Analog Converter using R-2R ladder and explain its working. Describe as to how the accuracy of the output voltage is obtained when the input voltages for binary bits are within certain ranges. 10

(b) Define percentage resolution of a DAC. Find the percentage resolution of a 10bit DAC which has a step size of 10 mV. 5

8. (a) Define Fan out, Propagation delay and Noise margin for logic families. 6

(b) Draw the circuit diagrams of TTL NAND gate and CMOS NOR gate. 9