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S. No. of Question Paper : 8335

Unique Paper Code : 234361

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Name of the Paper : CSPT-303 Computer Science-III (Computer System Architecture)

Name of the Course : B.Sc. (Physical Sciences)/B.Sc. (Mathematical Sciences)

Semester : III

Duration : 3 Hours

Maximum Marks : 75

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question No. 1 is compulsory.

Attempt any five questions from Question Nos. 2 to 8.

1. (a) Give the truth table of the expression $(A + AB')$. 2
- (b) Simplify the following expressions using Boolean algebra : 2
 - (i) $AB + AB'$
 - (ii) $A'B + ABC' + ABC$
- (c) How many address lines and input-output data lines are needed in a memory unit of size $2K \times 16$. 2
- (d) Represent decimal number 258 in : 2
 - (i) BCD
 - (ii) As a binary number.
- (e) Represent the binary number $(+1001.11)_2$ as a floating-point binary number having normalized mantissa of 8 bits and positive exponent of 6 bits. 2
- (f) Represent the following conditional control statement by the register transfer statement with control function :
if $(P = 1)$ then $(R1 \leftarrow R2)$ else if $(Q = 1)$ then $(R1 \leftarrow R3)$ 2

P.T.O.

- (g) Give the name and function of the following registers used in the Basic Computer :
AC and DR. 2
- (h) What is selective set operation ? Which logic microoperation can be used to represent it ? 2
- (i) Write control functions and microoperations required to execute ISZ instruction in the basic computer. 2
- (j) Give any *two* characteristics of CISC architecture. 2
- (k) What is the purpose of I/O Interface ? 2
- (l) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register ? 3
2. (a) Simplify the Boolean function F together with don't care condition d in : 6
- $$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 6, 8, 10)$$
- $$d(A, B, C, D) = \Sigma(4, 7, 9, 13)$$
- (i) Sum of products form
- (ii) Product of sums form
- (iii) Draw the logic diagram of simplified F.
- (b) Construct a 5-to-32 line decoder with block diagrams of four 3-to-8 line decoders with enable and one 2-to-4 line decoder. 4
3. (a) A two word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W+1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is :
- (i) Direct
- (ii) Immediate
- (iii) Relative
- (iv) Indexed. 4
- (b) Draw the digital circuit along with function table for 4-bit Bidirectional shift register with parallel load. 6

4. (a) Given the following expression :

6

$$X = A*B + C*D + E*F$$

Write the required sequence of steps needed to evaluate above expression using :

- (i) Three address instruction
 - (ii) Two address instruction
 - (iii) Zero address instruction
- (b) Design a logic diagram that performs the four logic operations : Exclusive-OR, Exclusive-NOR, NOR and NAND. Use two selection variables. 4
5. (a) The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E and I at the end of the ADD Indirect instruction. 6
- (b) Draw a logic diagram of bus system for four registers of 1 bit each using three state buffers and a decoder. 4
6. (a) Perform the arithmetic operation $(+75) + (+85)$ and $(-75) + (-85)$ with binary numbers in signed-2's complement representation. Use eight bits to accommodate each number together with its sign. Show that overflow occurs in both cases, that the last two carries are unequal, and that there is a sign reversal. 6
- (b) The 8-bit registers AR, BR, CR, and DR initially have the following values :

AR = 11110010

BR = 11111111

CR = 10111001

DR = 11101011

Determine the 8-bit values in each register after the execution of the following sequence of microoperations :

- (i) $AR \leftarrow AR + BR$
- (ii) $CR \leftarrow CR \wedge DR, BR \leftarrow BR + 1$
- (iii) $AR \leftarrow AR - CR$
- (iv) $DR \leftarrow DR \vee CR.$

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7. (a) Explain with example the four different types of I/O command that an interface may receive. 4
- (b) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts : an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
- (i) What is the size of Instruction Register ? 1
- (ii) How many bits are there in the operation code, the register code part and the address part ? 3
- (iii) How many bits are there in the data and address lines of the memory ? 2
8. Write short notes on the following : 5×2
- (a) DMA
- (b) Interrupt cycle.