This question paper contains 2 printed pages.

Roll No._____

Sr. No. of Question Paper: 1756
Unique Paper Code: 234 1102
Name of the Course: **B. Tech. (Computer Science) Semester-I** F-3
Name/ Title of the paper: **Computer System Architecture (CSDC1-102)**
Duration: **03 Hours** Maximum Marks: **75**

Question 1 is compulsory. Attempt any four questions from question numbers 2 to 7.

SECTION-A

1. (a) What is a flip flop? Draw the block diagram and write the truth table of an SR flip flop. (1+2+2)

   (b) Differentiate between an *encoder* and a *decoder*. Construct a 3 × 8 decoder with 2 × 4 decoders. (5)

   (c) Simplify the given Boolean expression: $x'z' + y'z' + yz' + xy$ and draw its circuit. (5)

   (d) What is a BSA instruction? Write down the sequence of micro-operations illustrating the execution of BSA. (5)

   (e) Write a symbolic micro program for fetching and execution of an ADD instruction. (5)

   (f) A computer system uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code that specifies one of 64 registers and an address part.

      i) How many bits are there in the operation code, register field and the address field? (2)

      ii) Draw the instruction word format and indicate the number of bits in each part. (2)

      iii) How many bits are there in the data and address inputs of the memory? (1)

   (g) What is the principle of locality of reference? How does it benefit the system? (2+3)

SECTION-B

2. (a) Give the truth tables of half and full adders. Derive the Boolean function of a full adder using Karnaugh Map. Hence draw its circuit diagram. (2+2+2)

   (b) The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case? (i) 2K × 16 (ii) 64K × 8 (iii) 16M × 32 (iv) 4G × 64 (1x4)

3. (a) List the micro operations for executing AND, SPA and INP instructions. (6)

(b) A digital computer has a memory unit with a capacity of 16, 384 words of 40 bits each. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no mode bit present). Two instructions are packed in one memory word and a 40 bit Instruction Register (IR) is available in the fetching and executing an instruction for this computer. (4)

4. (a) Explain the organization of a micro programmed control unit with the help of a block diagram. (5)

(b) An instruction stored at location 206 with its address field at location 207. The address field has value 720. A processor register R1contains the number 500. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with R1 as the index register. (5)

5. (a) Differentiate between programmed I/O and interrupt driven I/O. What is the advantage of DMA over these two techniques? (4+2)

(b) Name the two types of I/O channels? Explain each of them with the help of diagrams. (1+3)

6. (a) What is Reverse Polish notation? How is it beneficial in stack implementation? (1+1)

(b) Convert the following arithmetic expressions from infix to Reverse Polish notation:

i) A*B+C*D+E*F ii) A+B*[C*D+E*(F+G)] (2x2)

(c) Using De-Morgan theorem, show that:

i) $(A + B)'(A' + B')' = 0$ ii) $A + A'B + A'B' = 1$ (2x2)

7. (a) Explain direct mapping in cache with the help of an example. What are its advantages and disadvantages? (4+2)

(b) A set associative cache consists of 64 line, or slots, divided into four-line sets. A main memory unit contains 4K blocks of 128 words each. Show the format of the main memory address. (4)