This question paper contains 5 printed pages.

3263 *Your Roll No.* .....

B. Tech. (M) / II **J**

Paper II— ELECTRONICS

(EME–202)

Time : 3 hours *Maximum Marks* : 70

(Write your Roll No. on the top immediately on receipt of this question paper.)

Q. No. 1 is compulsory. Answer any four questions from the rest.

Assume any missing data suitably.

1. (*a*) Differentiate between Avalanche and Zener breakdown in diodes.

   (*b*) Why do you give DC bias for a transistor amplifier circuit?

   (*c*) Why do we prefer common collector configuration as last stage of cascaded amplifiers?

   (*d*) 'The input resistance of JFET is high.' Is it true or false? Justify your answer.

   (*e*) Explain virtual ground concept with respect to an operational amplifier.

   (*f*) Make a full adder using half adders and a gate. Explain its working with the help of a neat diagram.

P. T. O.

(*g*) Preset and clear inputs of a flipflop are said to be asynchronous inputs. Why. 7×2=14

2. (*a*) In a full wave rectifier the coltage applied to each diode is 240 sin 377*t*, the load resistance R_L = 2 k Ω and each diode has a forward resistance of 40 Ω. Determine the following:

(*i*) Peak value of current

(*ii*) DC value of current

(*iii*) Rms value of current

(*iv*) Rectifier efficiency

(*v*) Ripple factor

(*v*) Output ripple frequency. 7

(*b*) Draw the output waveform and transfer characteristics of the circuit shown in fig. 1. 3

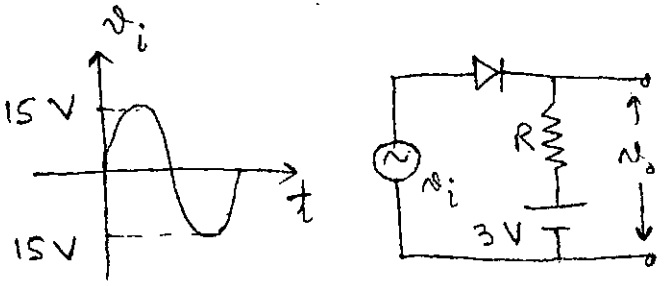

Fig.1

(*c*) The Zener diode shown in fig. 2 has a fixed voltage drop of 18 V across it so long as the Zener current is maintained between 200 mA and

2 amp. (*i*) Find the value of R so that the load voltage remains 18 V as input voltage is free to vary from 22 V to 28 V. (*ii*) Find the maximum power dissipated by the Zener diode. 4

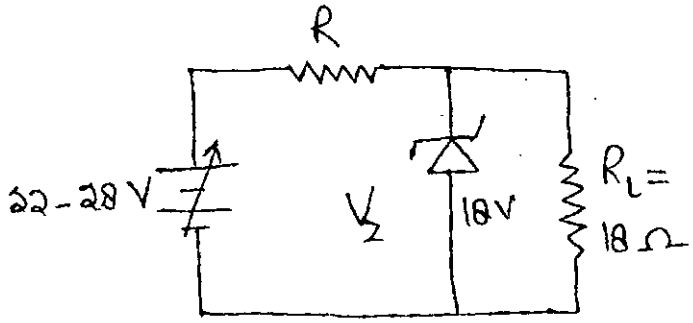

Fig. 2

3. (*a*) With the help of a neat diagram explain the output characteristics of common emitter configuration in detail. 4

(*b*) Find I_C and V_{CE} for the circuit shown in fig. 3. What happens to V_{CE} if β increases due to temperature? 7

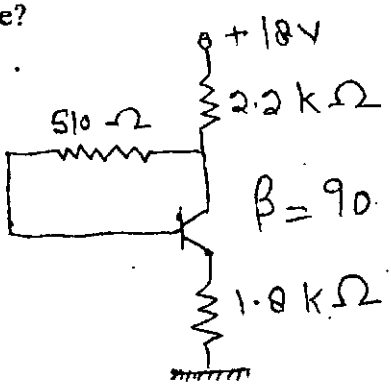

Fig. 3

P. T. O.

(*c*) Explain thermal runaway and how it is removed using voltage divider biasing circuit. 3

4. (*a*) An *n*-channel JFET has $V_P = -4$ V and $I_{DSS} = 10$ mA. It is used in circuit shown in fig. 4 with $V_{DD} = +12$ V. Determine the value of R_D and R_S so that $I_D = 3$ mA and $V_{OS} = 5$ V. 7

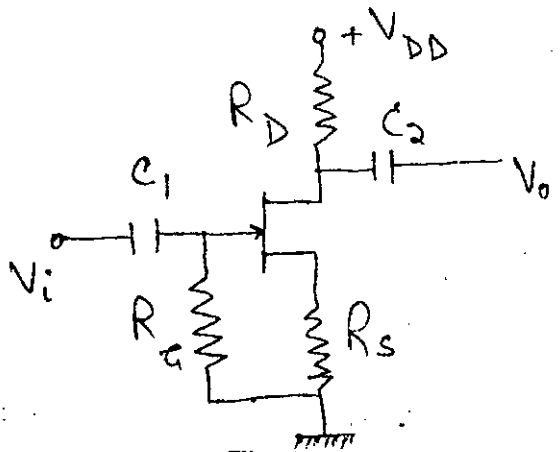

Fig. 4

(*b*) Discuss the advantages of regative feedback in amplifier. 4

(*c*) The voltage gain of an amplifier without feedback is 2000. Calculate the voltage gain of the amplifier if negative feedback is introduced in the circuit. Assume feedback factor as 0·01. 3

5. (*a*) A common emitter transistor amplifier circuit has the following characteristics: $h_{ie} = 1000\ \Omega$, $h_{fe} = 50$, $h_{re} = 2{\cdot}5 \times 10^{-4}$, $h_{oe} = 25 \times 10^{-6}$ A/V. If the load resistance $R_L = 10$ kΩ and source resistance is

100 Ω, find input resistance, output resistance, and the voltage, current and power gain. 7

(*b*) With the help of a neat circuit diagram, explain the working of a Wien bridge oscillator. Derive the expression for frequency of oscillations and condition for sustained oscillations. 7

6. (*a*) With the help of neat diagrams explain the working of Op-Amp based integrator and differentiator. Derive the respective equations for output voltage. 7

(*b*) Explain the working of a class B push-pull power amplifier. 7

7. (*a*) With the help of a neat diagram explain the working of a 4 input odd parity checker. 5

(*b*) Minimize:

$F(ABCD) = \sum m(1, 3, 7, 11, 15) + d(0, 2, 5)$ 5

(*c*) Prove that $\overline{A}\overline{B}\overline{C}+\overline{B}\overline{C}\overline{D}+AD=AD+\overline{B}\overline{C}$ 4

8. Write short notes on any *two*:

(*i*) SCR as a full wave controlled rectifier

(*ii*) Frequency response of RC coupled amplifier

(*iii*) Working of an enhancement MOSFET

(*iv*) 555 timer. 2×7=14

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