This question paper contains 4 printed pages.

3341 *Your Roll No.....*

B.Tech. (EEC) / I1
(P/T)
Paper V - DIGITAL CIRCUITS
(EEC - 205)

J

Time : 3 hours *Maximum Marks :70*

(Write your Roll No. on the top immediately on receipt of this question paper.)

Attempt any five questions.
Attempt all parts of a question in continuity.

1. a) Consider the following function :

$$F(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$$

Using Quine - McClusky method, determine :

(i) All prime implications
(ii) Essential prime implicants
(iii) The minimum SOP form. *07*

b) Using the method of map-entered variables, use 4 - variable maps to find a minimum sum-of-products expression for

$$Z(A, B, C, D, E, F, G) = \sum m(2, 5, 6, 9) + \sum d(1, 3, 4, 13, 14) + E(m_{11} + m_{12}) + F(m_{10}) + G(m_0)$$

07

2 a) Design a combinational circuit which has four inputs (A, B, C, D) and three outputs (X, Y, Z). XYZ

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represents a binary number whose value equals the number of 1's at the input (e.g. if ABCD = 1011, XYZ = 011) *07*

b) Design a circuit which will either subtract X from Y or Y from X, depending on the value of A. If A = 1, the output should be X - Y, and if A = 0, the output should be Y - X. Use a 4-bit subtractor and two 4-bit 2-to-1 multiplexers. *07*

3 a) Design a BCD adder circuit using 4 - bit adders. *07*

b) Design an 8 - to - 3 priority encoder using two 4 - to - 2 priority encoders and additional gates. *07*

4 a) What is Totem - pole output in TTL ? How does it speed - up the response ? *04*

b) Draw the circuit for CMOS NAND gate. Which special CMOS circuit has no TTL or ECL counterpart ? *04*

c) Draw the circuit for ECL OR/NOR gate and explain its working. Can we use ECL and TTL ICs in the same digital circuit ? *06*

5 a) Design a register incorporating four multiprocessors and four positive - edge - triggered D flip-flops having the behaviour specified in table below :

Select lines S_1	S_0	Register operation
0	0	Hold
0	1	Synchronous clear
1	0	Complement contents
1	1	Circular shift right.

06

b) Design a synchronous decade counter. *08*

6 a) Draw the circuit and explain the working of successive approximation Analog to digital converter. *05*

b) Define the following parameters of DACs
(i) Resolution
(ii) Accuracy
(iii) Linearity error
(iv) Settling time
(v) Offset voltage *05*

c) A dual slope A/D converter has a resolution of 8 - bits. If the clock rate is 100kHz, what is the maximum rate at which samples can be converted ? *04*

7 a) Draw the circuit diagrams of static RAM cell and Dynamic MOS RAM cell. Indicate Read and Write cycle timing in the timing diagram of SRAM. *09*

b) Using a PROM of an appropriate size, draw the logic diagram in PLD notation for a PROM realization to convert 4 - bit binary numbers into Gray code. *05*

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