[This question paper contains 4 printed pages.]

Sr. No. of Question Paper : 1570 **F-3** **Your Roll No.....**

Unique Paper Code : 2511301

Name of the Course : **B.Tech Electronics**

Name of the Paper : Digital System Design

Semester : III

Duration : 3 Hours Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Question number 1 is compulsory.
3. Attempt **five** questions in all.
4. Use of non-programmable scientific calculator is allowed.

1. (a) Convert the decimal number -54.75_{10} into its equivalent binary, octal and hexadecimal number. (3)

   (b) Perform the binary multiplication $1101.01_2 \times 101_2$. (3)

   (c) Draw the circuit diagram for a 2 bit binary adder/subtractor circuit which adds two binary numbers when $\overline{ADD}/SUB$ control line is low and subtracts the two numbers when $\overline{ADD}/SUB$ control line is high. What will be the output of the circuit if $\overline{ADD}/SUB$ is at logic 0 and the two input binary numbers are 01_2 and 10_2? (3)

P.T.O.

(d) What is race around condition ? In which Flip Flop is it observed and how can it be removed ? (3)

(e) Differentiate between SRAM and DRAM. (3)

2. (a) Draw the circuit diagram of TTL NOR gate and explain its working. (7)

(b) Explain with diagrams the current sourcing and sinking when two standard TTL gates are connected. (4)

(c) Subtract 77.64_{10} from -55.32_{10} using 2's compliment system of binary number representation with 8 bits in the integer part and 4 bits in the fractional part. Express your binary result in decimal form. (4)

3. (a) The message below has been coded in the 7 bit Hamming Code with ODD Parity. It is transmitted through a noisy channel. Decode the message assuming that at most single errors can occur.

0000001, 0011110 (5)

(b) Simplify the function using K maps and implement the circuit using NOR gates only.

F = B'DE' + A'BE + B'C'E' + A'BC'D'

d = BDE' + CD'E' (7)

(c) Give the circuit diagram and truth table of a full subtracter. (3)

4. (a) Construct a 5 to 32 decoder with four 3 to 8 decoders and a 2 to 4 decoder. Use block diagram construction. (5)

(b) Implement the function using 8 × 1 MUX

$F = \sum m(0, 1, 2, 3, 4, 10, 11, 14, 15)$ (5)

(c) Minimize the function using Boolean Algebra in POS as well as SOP form.

F = B D E + B' C' D + C D E + A' B' C E + A' B' C + B' C' D' E' (5)

5. (a) Using excitation table, explain how can, a SR flip flop be converted to a JK flip flop. (5)

(b) Draw and explain (using data) the working of a 4 bit bidirectional shift register using Mode as the control signal. Mode = 0 signifying shift left and Mode = 1 signifying shift right operation. (7)

(c) How can a Mod 6 up counter be implemented using Mod 3 and Mod 2 up counters. Explain with appropriate waveforms. (3)

6. (a) Design a synchronous MOD 11 down counter using JK flip flops. Draw its circuit diagram. (12)

(b) Which are the asynchronous inputs in a Flip Flop ? Why are these inputs called overriding inputs ? Explain using an SR flip flop. (3)

7. (a) Draw the PL A circuit architecture having 3 inputs, 4 outputs and 8 product terms which is programmed to implement

F1 = A'BC + AC' + AB'C

F2 = A'B'C + BC (6)

(b) Design a diode matrix ROM (16×1 using 2 dimensional addressing) for implementation of a logic function corresponding to

$$Y = \sum m(0, 2, 6, 7, 9, 12, 14, 15) \quad (6)$$

(c) Explain the difference between sequential access memory and random access memory. (3)