[This question paper contains 2 printed pages.]

Sr. No. of Question Paper : 1590 F-3 **Your Roll No.....**

Unique Paper Code : 2511304

Name of the Course : **B.Tech Instrumentation**

Name of the Paper : Digital Electronics

Semester : III

Duration : 3 Hours Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Use of scientific calculator is allowed.
3. Question No. **1** is compulsory.
4. Attempt any five questions in all.

1. (a) Subtract $7B_{16}$ from $C4_{16}$ using two's complement method of subtraction. (3)

   (b) Find the complement of the function f = (AB + CD) and show that f.f' = 0. (3)

   (c) Realize a full subtractor using a 3-line-to-8 line decoder. (3)

   (d) Find the characteristic equation for T flip flop. (3)

   (e) What is the difference between PROM, PAL and PLA ? (3)

2. (a) Explain the working of a two input TTL NAND gate with the help of circuit diagram. (7)

   (b) Explain working of a NMOS inverter. (4)

   (c) Define (i) Fan-in (ii) Noise Margin (4)

3. (a) Use the tabular method to simplify the given expression
   $F(V,W,X,Y,Z) = \Sigma m(0, 4, 12, 16, 19, 24, 27, 28, 29, 31)$ (7)

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(b) Design a Combinational logic circuit with four inputs A, B, C, D that will produce output '1' only whenever two adjacent input variables are 1s. A and D are also to be treated as adjacent. Implement it using NOR logic. (5)

(c) Implement a 16 × 1 MUX using two 8 × 1 MUXs and one 2 × 1 MUX. (3)

4. (a) Design a 3 bit gray to binary code converter. (5)

(b) Simplify the following Boolean expression to a minimum number of literals using (a) Boolean Laws (b) K-map
AB + AC′ + C + AD + AB′C + ABC (5)

(c) Draw the logic diagram and state table of a 3-bit Johnson's counter using D flip flop. Assume all the flipflops are reset initially. (5)

5. (a) Design a 3 bit ripple Up-counter using positive edge triggered J-K flip flop. (6)

(b) Draw the circuit of a 4 bit parallel-in, serial-out shift register using D flip-flop. (5)

(c) Explain with the help of a block diagram how a D-flip flop may be obtained from S-R flip flop. (4)

6. (a) Design a type D counter that goes through the states 0, 1, 2, 4, 0..... The unused states must always go to zero (000) on the next clock pulse. (8)

(b) State the truth table and also draw the logic diagram of a Octal - to – binary encoder. (4)

(c) Convert $(247.36)_8$ to equivalent hexadecimal number. (3)

7. (a) Differentiate between static RAM and dynamic RAM. (5)

(b) Explain how data is stored in magnetic bubble memory. (5)

(c) A certain memory has a capacity of 8K × 16.
(i) How many data input and data output lines does it have ?
(ii) How many address lines does it have ?
(iii) What is its capacity in bytes ? (5)