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Sr. No. of Question Paper	:	**1441**	**F-7**	**Roll No:.....**
Unique Paper Code	:	2511301		
Name of the Course	:	**B. Tech. Electronics**		
Name of the Paper	:	Digital System Design		
Semester	:	III		
Duration	:	3 hour		

Maximum Marks: 75

Instructions for Candidates

1. Write your Roll. No. on the top immediately on receipt of this question paper
2. Attempt five questions in all, including Q. No. 1 which is compulsory

1 (a) Perform the following conversion
(i) $4AB.2A_{16}$ to $(\ )_{10}$
(ii) 562.3_{10} to $(\ )_8$
(iii) 136_{10} to BCD

(b) Perform the following arithmetic operations
(i) 10011_2 - 11100_2 using 2's complement
(ii) $F25CF_{16} - 9BAC4_{16}$
(iii) $7320_8 + 32652_8$

(c) What is the difference between a combinational circuit and a sequential circuit? Give one example of each.

(d) Differentiate between volatile and non-volatile memory

(e) Define the following terms
(i) Fan-out
(ii) Propagation delay

3 x 5 =15

2 (a) $\overline{[A\overline{B}(A+C)+\overline{A}B(\overline{A+\overline{B}+\overline{C}})]}$ 5

Simplify the above expression using Boolean Algebra technique and realize the minimized circuit using NAND gates.

(b) Encode data bits 0101into the 7-bit even parity Hamming code. 5

P.T.O.

(c) With the help of diagram, explain the working of two-input TTL NAND gate 5

Q3 (a) Reduce the following function using K-map 5
$F = \sum_m (2,3,5,7,9,11,12,13,14,15)$

(b) A majority function is generated in a combinational circuit where the output is equal to 1 if the input variables have more 1's than 0's. The output is zero otherwise. Design a 3-input majority function. 5

(c) Design a 4 -bit binary Parallel Adder/Subtractor circuit. 5

Q4 (a) Making use of appropriate multiplexer implement the following logic function. 5
$A\bar{B}\bar{C}\bar{D} + \bar{A}BCD + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C + \bar{A}BC$

(b) Design a 4-input priority encoder with input D_0 having the highest priority and input D_3 the lowest priority. 5

(c) Implement the full adder circuit with a decoder circuit. 5

Q5 (a) What is a difference between latch and flip-flop? Show how an SR flip-flop can be converted into a D flip flop. 4

(b) Explain with diagram the operation of a universal shift register. 6

(c) Explain the 4-bit Ring counter 5

Q6 (a) A sequential circuit has two JK flip-flops, A and B; two inputs, x and y; and one output, z. The flip-flop input functions and the circuit output function are as follows: 8

$JA = Bx + \bar{B}\bar{y}$ $JB = \bar{A}x$

$KA = \bar{B}\bar{x}\bar{y}$ $KB = A + x\bar{y}$

$z = Axy + B\bar{x}\bar{y}$

(i) Draw the logic diagram of the circuit
(ii) Tabulate the state table
(iii) Derive the next-state equations for A and B

(b) What is modulus of a counter? Design a synchronous MOD-6 counter using T-flip flop 7

Q7 (a) Compare between synchronous and asynchronous counter? Design a 2-bit asynchronous up-counter. 5

(b) How many address lines, input/output data lines are needed to implement the following memory units 3

i) 4K x 16

ii) 16M x 32

lso give number of bytes stored in them

(c) Implement the following function in PLA 7

$$F1(A,B,C) = \sum(0,1,2,4)$$

$$F2(A,B,C) = \sum(0,5,6,7)$$