[This question paper contains 2 printed pages.]

Sr. No. of Question Paper : 2331 **F–4** **Your Roll No.....**

Unique Paper Code : 2511401

Name of the Course : **B. Tech. Electronics**

Name of the Paper : Analog Electronics – II

Semester : IV

Duration : 3 Hours Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Attempt **five** questions in all.
3. Question No. **1** is compulsory.
4. Use of Scientific calculator is allowed.

1. (a) List six characteristics of ideal op-amp. (3)

   (b) What are the limitations of basic op-amp differentiator ? Draw the circuit of practical differentiator. (3)

   (c) How fast the output of an op-amp changes by 10V, if its slew rate is 1V/μS. (3)

   (d) What is the concept of virtual ground in an op-amp ? (3)

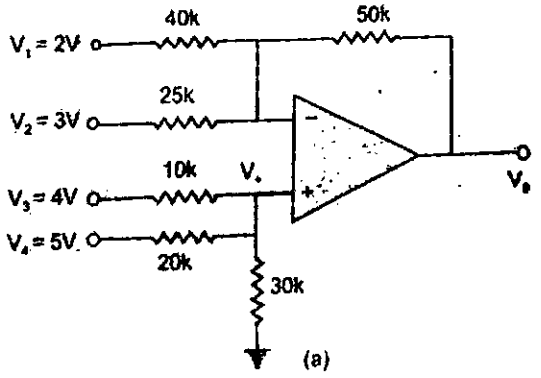
   (e) State and derive the conditions of sustained oscillations. (3)

2. (a) Explain Dual Input Balanced Output Differential Amplifier using AC and DC analysis. Determine differential voltage gain, differential input resistance and output resistance. (8)

   (b) Design a dual-input, balanced-output differential amplifier with a constant bias (using diodes) to satisfy the following requirements : Differential voltage gain $A_d = 40$, Current supplied by the constant current bias circuit = 4 mA, Supply voltages $V_s = \pm 10V$. (4)

   (c) Define CMRR. Derive expression for CMRR. (3)

3. (a) Find V_0 for adder-subtractor shown in Figure below. (4)



(b) Explain the working of Integrator circuit using basic and practical circuit approach. (6)

(c) How does high frequency model differ from the equivalent circuit operational amplifier ? Explain the effect of negative feedback on frequency response. (5)

4. (a) What is comparator ? Discuss using Zero and Level detector circuit. (4)

(b) Draw the circuit of square wave generator circuit. Explain its operation. (6)

(c) Give the block diagram of IC 566 VCO. Explain its operation. (5)

5. (a) Draw and explain the functional diagram of 555 timer. Derive the expression for time delay in monostable multivibrator circuit. (5)

(b) Design an astable multivibrator to generate a waveform of duty cycle of 0.25 and 0.5. (5)

(c) What is PLL ? Explain its operating principle. (5)

6. (a) Derive the expression for cutoff frequency of second order Low pass filter. (7)

(b) Draw and explain the circuit of Log amplifier. Derive the expression of output voltage. (4)

(c) Design a wide band-pass filter with f_L = 400 Hz, f_H = 2 kHz, and passband gain = 4. (4)

7. (a) Design phase shift oscillator for a cutoff frequency of 1 KHz. (5)

(b) What is voltage limiter circuit ? Support the answer with a circuit diagram and necessary waveforms. (5)

(c) Design first order high pass filter with a cutoff frequency of 2 KHz and a passband gain equal to 1. (5)

(700)