## B. Tech. (EC) / IV

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## Paper EEC-404 (f).

## FAULT TOLERANT COMPUTING

Time: 3 hours

Maximum Marks: 70

(Write your Roll No. on the top immediately on receipt of this question paper.)

Attempt any five questions.

All questions carry equal marks.

- (a) What are the types of fault generated in TTL NAND gate if signal line open, supply voltage open, ground open, signal line and V<sub>CC</sub> short-circuited, signal line and ground short-circuited? Draw a neat diagram of a TTL NAND gate and explain these in details.
  - (b) What do you mean by 'stuck-open faults' in CMOS NOR gate? Explain the same by drawing a neat diagram of CMOS NOR gate.
- 2. (a) Explain the concept of dynamic redundancy for hardware fault tolerance.
  - (b) Drawing a neat diagram of ESS, explain how BELL system of Telephone Laboratory incorporates hardware dynamic fault tolerance in the ESS.

- 3. (a) Explain the concept of signature analysis and the working of signature analyzer circuit. 8
  - (b) Calculate the period of 99% reliability for a first generation computer containing 8000 thermionic valves each with  $\lambda = 0.5\%$  (1000 hrs).
- 4. (a) Explain, by drawing a neat diagram, onedimensional path sensitization technique for the detection of faults in any combinational circuit. 8
  - (b) What do you know about the 'pulse-mode' and 'fundamental-mode' of operation of the synchronous sequential circuit. Explain also what you mean by a strongly connected sequential machine.
- 5. (a) For the following state table obtain an isomorphic reduced state table:

	Next States and Present Outputs			
Present States	x=0	<i>x</i> =1		
A	F, 0	C, 0		
В	H, 1	A, 1		
C	H, 0	D, 1		
D	B, 0	H, 0		
E	G, 0	C, 0		
F ·	C, 1	E, 1		
G	H, 1	E, 1		
Н	C, 0	A, 1		

(b)	Explain	what	you	mean	by s	ynchronizing
	sequence	for a	redu	iced, c	complete	ely specified
	sequentia	l mach	ine.	•		•

- What do you mean by the term BILBO? Draw its logic diagram. How are the BILBOs utilized in the formation of BIDCO? Explain the entire operation of a BILBO.
- 7. Write short notes on following:
  - (i) Self-checking checker circuits

Or

SPOOF method of Clegg for the fault detection in the combinational circuit 6

- (ii) 'Transition counting' method 4
- (iii) Syndrome testing for a circuit.

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